REMARKS

Applicants have carefully reviewed the office action dated September 27, 2004. This response is believed to address all grounds for rejection stated in the office action.

Attorney Docket Number

Please change the attorney docket number for this application to Larsson 29-19.

Amendments to Claim 7

Claim 7 is amended to clarify the invention. The language used in claim 7 is taken from the specification as used to describe FIG. 3. See Specification p. 4, lines 19-27. Accordingly, no new matter is added with this amendment. The Examiner is respectfully requested to review and enter the amendment.

Addition of New Dependent Claim

Claim 8, depending from independent claim 7 has been added. No new matter is added as a result of this claim. Support for this amendment is available in the Specification at page 4, lines 26-27. Examiner is requested to review and enter the amendment.

Rejection of claim 7 under 35 U.S.C. § 112, ¶¶ 1&2

Claim 7 is rejected under 35 U.S.C. § 112, ¶¶ 1 (enablement) & 2 (as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention). Applicants have amended claim 7 to clarify the features of the invention and to make it more readable. Because of the changes made, applicants respectfully request the Examiner to withdraw these rejections.

Rejection of claim 4 under 35 U.S.C. § 103(a) over Chiu

Examiner rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Chiu (USP 5,257,217). Applicants respectfully traverse this rejection on the following grounds. Claim 4 recites as follows.

4. (original) An apparatus for adding a plurality of partial products comprising:

a plurality of carry-save adders coupled together in series, each of the plurality of carry-save adders receiving a successive one of the plurality of partial products and two intermediate vectors (In-1, In-2) from a prior carry-save adder in the series of carry-save adders and each of the plurality of carry-save adders outputting a carry bit (Cn-1) a sum bit (Sn-1) and two intermediate vectors (In, In+1) wherein a first one in the series of carry-save adders receives two of the plurality of partial products;

a last carry-save adder coupled to a last one in the series of carry-save adders, receiving a last one of the plurality of partial products and two intermediate vectors from said last one in the series of carry-save adders, and outputting a plurality of sum bits and a plurality of carry bits; and

a plurality of half-adder/full-adder series combinations coupled to the last carry-save adder, each of the plurality of half-adder/full-adder series combinations receiving two carry bits of the plurality of carry bits output by the last carry-save adder and two sum bits of the plurality of sum bits output by the last carry-save adder, and outputting two result bits and a carry bit.

Examiner states that Chiu disclosed all features of the invention as claimed in claim 4. A difficulty in responding to this rejection is that the Office Action does not cite to the text in Chiu where there is similarity between the instant rejected claim 4 and Chiu. It is submitted that Chiu does not disclose or teach any part of the rejected claim 4. For instance, Chiu does not teach or suggest the features claimed in claim 4, which is described in the specification with respect to FIG. 6 as follows.

If some speed degradation is acceptable, some of the Cmsb and Smsb bits can also be reduced. One such implementation 60 is shown in FIG. 6, which saves 25% of the registers, as each group

of four bits is reduced to three. For example, bits s7, c6, s6 and c5 are converted to bits c7a, r7 and r6, respectively, by adders 43 and 42. Adder pairs 44, 45 and 46, 47 perform similar functions for their inputs. The adder pairs repeat depending upon the length of the multiplier 60. The last two three bits output by carry-save adder 36 are the sum bit s36, carry bit c36 and carry bit c35, which are converted into c37a, r37 and r36 by adders 46, 47 as shown in FIG. 6.

As shown in FIG. 6, the registers 49a, 49b of FIG. 3, are replaced with adders 41-47, and a single output register 65. Output register 65 can be either a single register, combining registers 49a, 49b and 48 or two registers, one for the least significant bits, such as register 48, and another for the most significant bits. The output of the adders 41-47 are fed into the single MSB output register 65, thereby reducing the number of registers by at least one for each stage. The inputs to the adders 41-47 are from the carry-save adders 35 and 36 as shown in FIG. 6. The inputs to adders 37-40 remain as shown in FIG. 3. Thus, bit r5 comes directly from adder 41 and carry bit c5a also comes from adder 41. The output from half-adder 42 is r6. The output from full-adder 43 is bit r7 and carry bit c7a. At the end of the register, the output from half-adder 47 is r37 and a carry bit c37a; and the output from half-adder 46 is r36. The output from full-adder 45 is carry bit c35a, and result bit r35. Result bit r34 comes from half-adder 44. The half-adder/full adder combination repeats as shown in FIG. 6, depending upon the length of the multiplier 60. In a 32-bit multiplier, the end result is each 4-bit group output by carry-save adder 36 is converted into a 3-bit group and stored in a register, thereby reducing the number of bits in the register from a total of 64 bits (i.e., two registers 27, 28 times 32-bits stored in each register) to 48 bits (i.e., one register

storing 16 groups of 3-bits). Thus saving 25% of the memory requirements, for a small speed degradation.

Nothing in Chiu resembles FIG. 6. But claim 4 has many more detailed features recited which features are neither explicitly disclosed in Chiu nor would have been obvious to one of ordinary skill in the art at the time the invention was made. Examiner appears to have taken Official Notice that all designs of multiplier circuits would have "a plurality of carry save adders and a propagate adder [at the final stage]" (see office action at page 3, ¶ 4). Applicants respectfully request the Examiner to show the basis for taking such official notice. See M.P.E.P. § 2144.03; see also, *In re Lee*, 277 F.3d 1338, 1344-45, 61 U.S.P.Q. 2d 1430, 1434-35 (Fed. Cir. 2002) (holding that general conclusions concerning what is "basic knowledge" or "common sense" to one of ordinary skill in the art without specific factual findings and some concrete evidence in the record to support these findings will not support an obviousness rejection). In particular, focusing on the recitation in claim 4,

> a plurality of half-adder/full-adder series combinations coupled to the last carry-save adder, each of the plurality of half-adder/full-adder series combinations receiving two carry bits of the plurality of carry bits output by the last carry-save adder and two sum bits of the plurality of sum bits output by the last carry-save adder, and outputting two result bits and a carry bit

This feature is nowhere to be seen in Chiu. Examiner is requested to reconsider and withdraw this rejection.

Rejection of claims 1-4 under 35 U.S.C. § 103(a) over Weinberger

Examiner rejected claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over Weinberger (USP 4,463,439). Applicants respectfully traverse this rejection on the following grounds.

As to independent claim 1, Examiner admits that Weinberger did not specifically teach or describe the "output register." Nevertheless, the Examiner states that because Weinberger described that the "resulting bit" should be "stored in memory means," see office action at page 4, line 7, "it would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention

according to Weinberger's teachings because the reference discloses a multiplier circuit having a plurality of carry save adders and a propagate adder [at the final stage] as claimed." *Ibid.* Claim 1 recites as follows.

> 1. (previously amended) An apparatus for adding a plurality of partial products comprising:
>
> a plurality of carry-save adders coupled together in series, each of the carry-save adders in the series receiving one of the plurality of partial products and two intermediate vectors from a prior carry-save adder in the series of carry-save adders, and outputting a carry bit, a sum bit and two intermediate vectors, wherein the first one in the series of carry-save adders receives two of the plurality of partial products;
>
> a last carry-save adder coupled to a last one in the series of carry-save adders and receiving a last partial product of the plurality of partial products and two intermediate vectors from a last one in the series of carry-save adders, and outputting a carry vector (Cmsb) and a sum vector (Smsb);
>
> a plurality of carry-propagate adders coupled in series and coupled to the plurality of carry-save adders, each of said plurality of carry-propagate adders outputting a resulting bit and a carry bit; and
>
> an output register coupled to the first one in the series of carry-save adders, the last carry-save adder, and the plurality of carry-propagate adders, and storing the plurality of resulting bits, the sum bit output by the first one in the series of carry-save adders and the carry bit output by the last one in the series of carry-propagate adders.

Weinberger does not disclose or suggest a carry save adder. Nowhere in Weinberger is described a series of carry-save adders, a plurality of carry-propagate adders and an output register as described in the examined claim 1. Weinberger is directed toward a binary full adder stage from half-adder stages. See col. 1, lines 35-40.

Examiner cited the following text in support of the argument that Weinberger rendered claim 1 obvious.

> In FIG. 12, the 4x4 multiplier with the carry save adder tree uses the half and full adders described above. The tree accepts 4 bits each of the multiplicand and multiplier to produce the low order 4 bit product directly. The high order carry and sum bits are combined in a known propagate adder 26 to produce the high order 4 bit product. No additional gating is needed to produce the individual products of one multiplier by one multiplicand bit. Instead the bit products are implied by appropriate bundling of the input bits i.e. $a_i \ldots b_j$ enters in complement form as an OR bundle $a_i + b_j$.

It is respectfully submitted that Weinberger is not the same as the instantly examined claim 1. In fact, nowhere in Weinberger is there a series of carry-save adders and a set of carry-propagate adders with the additional features as claimed in claim 1. Examiner is requested to reconsider and withdraw the rejection.

Claims 2 and 3 are dependent on Claim 1 and incorporate the features of claim 1. Because it is shown that Weinberger does not render claim 1 obvious, as per the discussion above, the same argument is presented by reference to show that claims 2 and 3 would not have been obvious to one of ordinary skill in the art at the time the invention was made. Examiner is requested to reconsider.

As to claim 4, Examiner relies on the same cited paragraph with respect to FIG. 12 of Weinberger to argue that Claim 4 would have been obvious to one of ordinary skill in the art at the time the instant invention was made. However, as argued with respect to the Chiu reference, the key features of claim 4 include, among others, the following recitation:

> a plurality of half-adder/full-adder series combinations coupled to the last carry-save adder, each of the plurality of half-adder/full-adder series combinations receiving two carry bits of the plurality of carry bits output by the last carry-save adder and two sum bits of the plurality of sum bits output by the last carry-save adder, and outputting two result bits and a carry bit

This feature is nowhere present in Weinberger. Examiner is requested to show any basis if the Examiner takes official notice of the existence of this feature either in Weinberger or in the domain of common knowledge among persons of ordinary skill in the art at the time the invention was made. See M.P.E.P. § 2144.03. In the absence of any basis, it is respectfully submitted that Weinberger would not have taught or suggested to one of skill in the art to make the instant invention at the time the instant invention was made. Reconsideration is respectfully requested.

Conclusion

In view of the foregoing remarks and amendments, Applicants believe that all claims currently pending are patentable. No fee is believed to be due with this response. Reconsideration and an early notice of allowance are respectfully solicited.

Respectfully submitted,

Naren Chaganti (Reg. No. 44,602)
432 S. Curson Ave, Ste. 12 H
Los Angeles, CA 90036
naren@chaganti.com E-mail
(650) 248-7011 phone

Attorney for Applicants

Certificate of Faxing

The undersigned certifies that on the date shown below, the foregoing document was filed via fax with the USPTO by faxing the same to the telephone number (703) 746-7239.

Dated: 12-27-04

Naren Chaganti (Reg. No. 44,602)